WHAT IS CLAIMED IS:

1. A timing signal generating device for generating timing signals in accordance with set data, comprising:

a first setting circuit for outputting first set data to be used to generate the timing signals;

a second setting circuit for outputting second set data to be used to generate the timing signals;

a generating circuit for generating first timing signals in accordance with said first set data input from said first setting circuit; and

a controller for defining a timing for setting said second set data output from said second setting circuit in said generating circuit;

wherein said generating circuit generates second timing signals in accordance with said second set data input from said second setting circuit at the timing defined by said controller.

2. A device in accordance with claim 1, wherein said first setting circuit sets said first set data in said generating circuit when a system including said device is starts up.

3. A device in accordance with claim 1, further comprising:

a first transfer circuit for transferring said first set data to said generating circuit at a high speed; and

a second transfer circuit for transferring said second set data to said generating circuit at a speed lower than said first transfer circuit;

wherein said first setting circuit and said second setting circuit transfer said first set data and said second set data to said generating circuit via said first circuit

and said second circuit, respectively, causing said generating circuit to generate timing signals in accordance with said first set data or said second set data.

4. A device in accordance with claim 3, wherein said first transfer circuit comprises a parallel bus connected to said generating circuit, said first setting circuit outputting said first set data on the parallel bus.

5. A device in accordance with claim 4, wherein said first transfer circuit is connected to an output bus of a converting circuit that converts an analog signal to a digital value.

6. A device in accordance with claim 3, wherein said second transfer circuit comprises a serial bus, said second setting circuit outputting said second set data on said serial bus.

7. A device in accordance with claim 1, wherein said first timing signals represented by said first set data do not vary an operation of a system, which includes said device, under way.

8. A device in accordance with claim 1, wherein said second timing signals represented by said second set data vary an operation of a system, which includes said device, under way.

9. A timing signal generating device for generating timing signals in accordance with set data, comprising:

a setting circuit for selectively outputting first set

data or second set data to be used to generate the timing signals;

a generating circuit for generating timing signals to be used to drive an image pickup device, which generates pixel signals representative of an optical image;

a controller for defining a timing for setting said second set data in said generating circuit; and

a transferring circuit for selectively transferring said first set data or said second set data to said generating circuit and transferring the timing signals to the image pickup device;

wherein said setting circuit controls a direction of data transfer effected via said transferring circuit, and wherein said generating circuit generates first timing signals in accordance with said first set data output from said setting circuit, generates second timing signals in accordance with said second set data transferred at the timing defined by said controller, and selectively feeds said first timing signals or said second timing signals to the image pickup device, which is connected to said generating circuit via said transferring circuit.

10. A device in accordance with claim 9, wherein when said generating circuit feeds said first timing signals or said second timing signals to the image pickup device, said setting circuit controls an output of said setting circuit to a high impedance state.

11. A device in accordance with claim 9, wherein when said setting circuit outputs said first set data or said second set data, said setting circuit feeds a switching signal to said generating circuit to thereby switch an output of said generating circuit to an input.

12. A device in accordance with claim 11, wherein when said setting circuit outputs said first set data or said second set data, said setting circuit freezes the image pickup device.

13. A device in accordance with claim 9, wherein said setting circuit sets said first set data in said generating circuit when a system including said device is started up.

14. A device in accordance with claim 9, wherein said first timing signals represented by said first set data do not vary an operation of a system, which includes said device, under way.

15. A device in accordance with claim 9, wherein said second timing signals represented by said second set data vary an operation of a system, which includes said device, under way.

16. A method of generating timing signals in accordance with set data, comprising:

a first setting step of outputting first set data to be used to generate the timing signals;

a second setting step of outputting second set data to be used to generate the timing signals;

a generating step of generating first timing signals in accordance with said first set data output in said first setting step, and generating second timing signals in accordance with said second set data output in said second setting step; and

an outputting step of selectively outputting said first timing signals or said second timing signals output in said generating step;

wherein said first setting step outputs said first set data when a system using the timing signals is started up.

17. A method in accordance with claim 16, wherein said first timing signals represented by said first set data do not vary an operation of the system under way.

18. A method in accordance with claim 16, wherein said second timing signals represented by said second set data vary an operation of the system under way.

19. A method in accordance with claim 16, wherein said first setting step outputs said first set data at a high speed, said second setting step outputting said second set data at a speed lower than said first setting step.